



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/607,029	06/27/2003	Chang Wook Han	049128-5111	5609
9629	7590	11/17/2005	EXAMINER	
MORGAN LEWIS & BOCKIUS LLP 1111 PENNSYLVANIA AVENUE NW WASHINGTON, DC 20004			QUINTO, KEVIN V	
			ART UNIT	PAPER NUMBER
			2826	

DATE MAILED: 11/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/607,029

Applicant(s)

HAN, CHANG WOOK

Examiner

Kevin Quinto

Art Unit

2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 19 August 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-32 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1, 2, 4-6, 14-17, 19, 20, 28, 29 and 31 is/are rejected.
- 7) ☒ Claim(s) 3, 7-13, 18, 21-27, 30 and 32 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |   |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)                        | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)    | Paper No(s)/Mail Date. _____  |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____   | 6) <input type="checkbox"/> Other: _____                                    |

## **DETAILED ACTION**

### ***Response to Arguments***

1. Applicant's arguments filed August 19, 2005 have been fully considered but they are not persuasive. The examiner notes that newly amended claims 1 and 15 has deleted the phrase, "or formed between the substrate and the low refractive film" but still includes the limitation, "at least one low refractive thin film formed on the substrate; an organic electro luminescence diode formed on the low refractive thin film to selectively emit light; and a switching device formed on the low refractive thin film." The examiner would like to note that the use of the word "on" by itself does not necessarily mean direct contact between two objects or layers in the semiconductor art. The word "on" by itself could mean that there may possibly be one or several layers between the two objects or layers to which the word "on" is referring. The applicant appears to interpret the word "on" in the same manner since claims 1 and 15 describe "at least one low refractive thin film formed on the substrate" while the specification does not appear to disclose any embodiment in which the low refractive thin film is in direct contact with the substrate. Using this interpretation of "on," the Fujita reference (USPN 6,538,390 B2) still discloses embodiments which reject claims 1, 2, 4, 5, 14, 15, 16, 17, 19, 28, 29, and 31 under 35 USC § 102 as well as claims 6 and 20 under 35 USC § 103 in conjunction with Zhang (USPN 5,313,075).

### ***Claim Rejections - 35 USC § 102***

Art Unit: 2826

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 2, 4, 5, 14, 15, 16, 17, 19, 28, 29, and 31 are rejected under 35 U.S.C. 102(e) as being anticipated by Fujita et al. (USPN 6,538,390 B2).

4. In reference to claims 1 and 15, Fujita et al. (USPN 6,538,390 B2, hereinafter referred to as the "Fujita" reference) discloses a similar device and its method of fabrication. Figures 3(o), 5, 6, 7, and 9 each illustrate an active matrix organic electro luminescence display panel device with a low refractive film thin film (12) on the substrate (1). The examiner would like to note that the use of the word "on" by itself does not necessarily mean direct contact between two objects or layers in the semiconductor art. The word "on" by itself could mean that there may possibly be one or several layers between the two objects or layers to which the word "on" is referring. The applicant appears to interpret the word "on" in the same manner. The low refractive thin film (12) is made of silicon dioxide, a known low refractive film (see Kamijo – United States Patent Application Publication No. US 2002/0130991, p.1, paragraph 10). An organic electro luminescence diode (8) is formed on the low refractive thin film (12) to selectively emit light. A switching device (2), a transistor, with a gate (11) and an active layer (9), is formed on the low refractive film (12) in order to selectively drive the organic

electro luminescence diode (8). The method of fabricating the device of figures 3(o), 5, 6, 7, and 9 meets the claimed method described in claim 15 wherein an organic electro luminescence diode (8) is formed on the low refractive thin film (12) to selectively emit light. A switching device (2), a transistor, with a gate (11) and an active layer (9), is formed on the low refractive film (12) in order to selectively drive the organic electro luminescence diode (8). In the alternative interpretation of figures 3(0), 5, 6, 7, and 9, the switching device (2) or transistor, with a gate (11) and an active layer (9), is formed between the low refractive film (12) and the substrate (1) in order to selectively drive the organic electro luminescence diode (8).

5. With regard to claims 2 and 17, Kamijo states that silicon dioxide has a refractive rate (n) of 1.455. Thus the low refractive thin film (12) of Fujita inherently meets the claimed device and its method of fabrication.

6. In reference to claims 4 and 16, Fujita discloses (column 10, lines 41-58) the use of a capacitor formed on the low refractive thin film (12), for sustaining a light emission of the organic electro luminescence diode (8).

7. In reference to claims 5 and 19, the organic electro luminescence diode (8) of Fujita includes a first electrode (5) formed of a transparent conductive material (column 7, lines 29-32) formed on the low refractive thin film (12) and connected to the switching device. An organic light emission layer (61, 62) including an organic luminous material (62) is on the first electrode (5). A second electrode (7), which includes a metal material (column 12, lines 3-6), covers the organic light emission layer (61, 62), the switching device (2), and the capacitor.

Art Unit: 2826

8. In reference to claims 14 and 28, Fujita (USPN 6,538,390 B2) discloses a similar device and its method of fabrication. Figures 3(o), 5, 6, 7, and 9 each illustrate an active matrix organic electro luminescence display panel device with a low refractive film thin film (12) on the substrate (1). The examiner would like to note that the use of the word "on" by itself does not necessarily mean direct contact between two objects or layers in the semiconductor art. The word "on" by itself could mean that there may possibly be one or several layers between the two objects or layers to which the word "on" is referring. The applicant appears to interpret the word "on" in the same manner. The low refractive thin film (12) is made of silicon dioxide, a known low refractive film (see Kamijo – United States Patent Application Publication No. US 2002/0130991, p.1, paragraph 10). An organic electro luminescence diode (8) is formed on the low refractive thin film (12) to selectively emit light. The switching device (2) or transistor, with a gate (11) and an active layer (9), is formed between the low refractive film (12) and the substrate (1) in order to selectively drive the organic electro luminescence diode (8). In figures 3(o), 5, and 7, there is a first insulating layer (3) formed between the substrate (1) and the low refractive film (12) to cover the switching device (2). In figures 6 and 9, there is a first insulating layer (3 or 4) formed between the substrate (1) and the low refractive film (12) to cover the switching device (2). The method of fabricating the device of figures 3(o), 5, 6, 7, and 9 meets the claimed method described in claim 28.

9. With regard to claims 29 and 31, Kamijo states that silicon dioxide has a refractive rate ( $n$ ) of 1.455. Thus the low refractive thin film (12) of Fujita inherently meets the claimed device and its method of fabrication.

***Claim Rejections - 35 USC § 103***

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

11. Claims 6 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujita et al. (USPN 6,538,390 B2) in view of Zhang et al. (USPN 5,313,075).

12. In reference to claims 6 and 20, Fujita shows in figures 3(o), 5, 6, 7, and 9 that the switching device (2) on a glass substrate (1) which has a semiconductor layer (9) with a gate (11) and a gate insulating film (not labeled) sequentially deposited on it. A drain electrode (10) is connected to the semiconductor layer (9) and is connected to the first electrode (5) of the organic electro luminescence diode. A source electrode (13) is connected to the semiconductor layer (9). As shown in figure 10, the source of the transistor is connected to the capacitor (23) while its drain is connected to the organic electro luminescence diode (8). Fujita does not disclose forming a buffer layer between the switching device (2) and the substrate (1). However the use of a buffer layer is well known in the art. Zhang et al. (USPN 5,313,075, hereinafter referred to as the "Zhang" reference) discloses that using a buffer layer between a transistor and a glass substrate prevents unwanted diffusion of impurities from the glass substrate into the transistor (column 3, lines 3-17). The diffusion of impurities from a glass substrate into a transistor leads to poor device characteristics and lower long-term reliability (column 2,

lines 40-44). In view of Zhang, it would therefore be obvious to implement a buffer layer between the substrate and transistor or switching device of Fujita in order to gain the benefit of improved reliability.

### ***Allowable Subject Matter***

13. Claims 3, 7-13, 18, 21-27, 30, and 32 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

14. The following is a statement of reasons for the indication of allowable subject matter: the examiner is unaware of any prior art which suggests or renders obvious an active matrix organic electro luminescence display panel device with the explicit layer structure with regard to the low refractive thin film, the buffer layer and capacitor electrode as described the applicant.

### ***Conclusion***

15. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not



Art Unit: 2826

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Quinto whose telephone number is (571) 272-1920. The examiner can normally be reached on M-F 8AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



KVQ

**NATHAN J. FLYNN**  
**SUPERVISORY PATENT EXAMINER**  
**TECHNOLOGY CENTER 2800**